ABSTRACT OF THE DISCLOSURE

A semiconductor apparatus including programmability that may allow a SSTL interface or LVTTL interface is provided. A reference configuration circuit (**100**) may provide a primary reference potential VREF0 and secondary reference potential VREF. Reference configuration circuit (**100**) may include a bond pad (**PAD1**), a reference potential generation circuit (**1**), a control circuit (**50**), a reference selection circuit (**60**), and a secondary reference potential generation circuit (**70**). During a wafer test mode, primary reference potential VREF0 and secondary reference potential VREF may be provided from a potential that may be applied to bond pad (**PAD1**).